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Worst-case Stall Analysis for Multicore Architectures with Two Memory Controllers (Artifact)

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Abstract


This artifact demonstrates the performance of the proposed worst-case memory stall analysis for a memory-regulated multicore with two memory controllers. The memory stall analysis is implemented in Java along with five different stall-cognisant bandwidth-to-core and task-to-core assignment heuristics. It evaluates the performance of these heuristics in terms of schedulability via experiments with synthetic task sets capturing different system characteristics. It also quantifies the cost in terms of extra stall for letting all cores benefit from the memory space offered by both controllers on the given multicore platform.

Worst-case Stall Analysis for Multicore Architectures with Two Memory Controllers (Artifact)*

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Abstract

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these heuristics in terms of schedulability via experiments with synthetic task sets capturing different system characteristics. It also quantifies the cost in terms of extra stall for letting all cores benefit from the memory space offered by both controllers on the given multicore platform.

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Keywords and phrases multiple memory controllers, memory regulation, multicore

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1 Scope

The artifact allows to repeat and replicate the experiments with different system configurations. The provided tool can be reused and extended for further improvements in this line of work. This artifact demonstrates that worst-case memory stall analyses for single-memory-controller multicores with memory regulation are unsafe if applied to multicores with multiple memory controllers. It explores the performance of five different stall-cognisant bandwidth-to-core and task-to-core allocation heuristics (each specialising in optimising processing capacity and/or memory bandwidth) in terms of schedulability ratio with synthetic workload capturing variety of system characteristics. It further shows that the proposed memory-fit heuristic performs well if bandwidth is scarce. The even and uneven heuristics are suitable for balanced systems, while greedy-fit and humble-fit are handy for compute-intensive systems. The artifact also highlights the performance implications of having fully shared memory controllers vs. partitioning the controllers to different cores, in cases when the latter arrangement would be viable from the application perspective (i.e., no data sharing across memory domains).

2 Content

The artifact package includes:

- Super shell script
- Shell script wrapper
- Java tool
- Matlab scripts

The super shell script invokes several shell script wrappers, which in turn runs the Java tool and provides its required inputs. The Java tool implements our proposed algorithms (given in ECRTS paper) and generates the output data for the given set of inputs. All the scripts invoked by the super shell script complete their execution with output files. These output files are used by the Matlab script to analyse the data and generate results.

3 Getting the artifact

The artifact endorsed by the Artifact Evaluation Committee is available free of charge on the Dagstuhl Research Online Publication Server (DROPS). In addition, the artifact is also available at: https://drive.google.com/file/d/1y_mu10rRjHwS0JStRoVzEx7NiSky5m3F/view?usp=sharing.

4 Tested platforms

This artifact requires two software tools: a) Java (JDK) and c) Matlab. It can be configured both on Linux or Windows operating system.

5 License

The artifact is available under GNU General Public License (GPL), Version 2.0 (<https://www.gnu.org/licenses/gpl-2.0.html>)

6 MD5 sum of the artifact

8dfb457b3b359cb07fa51904d24c27cc

7 Size of the artifact

1.62 MB